Readout Electronics Design Considerations for LAr TPC

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On behalf of the Cold Electronics Team
May 11th, 2013

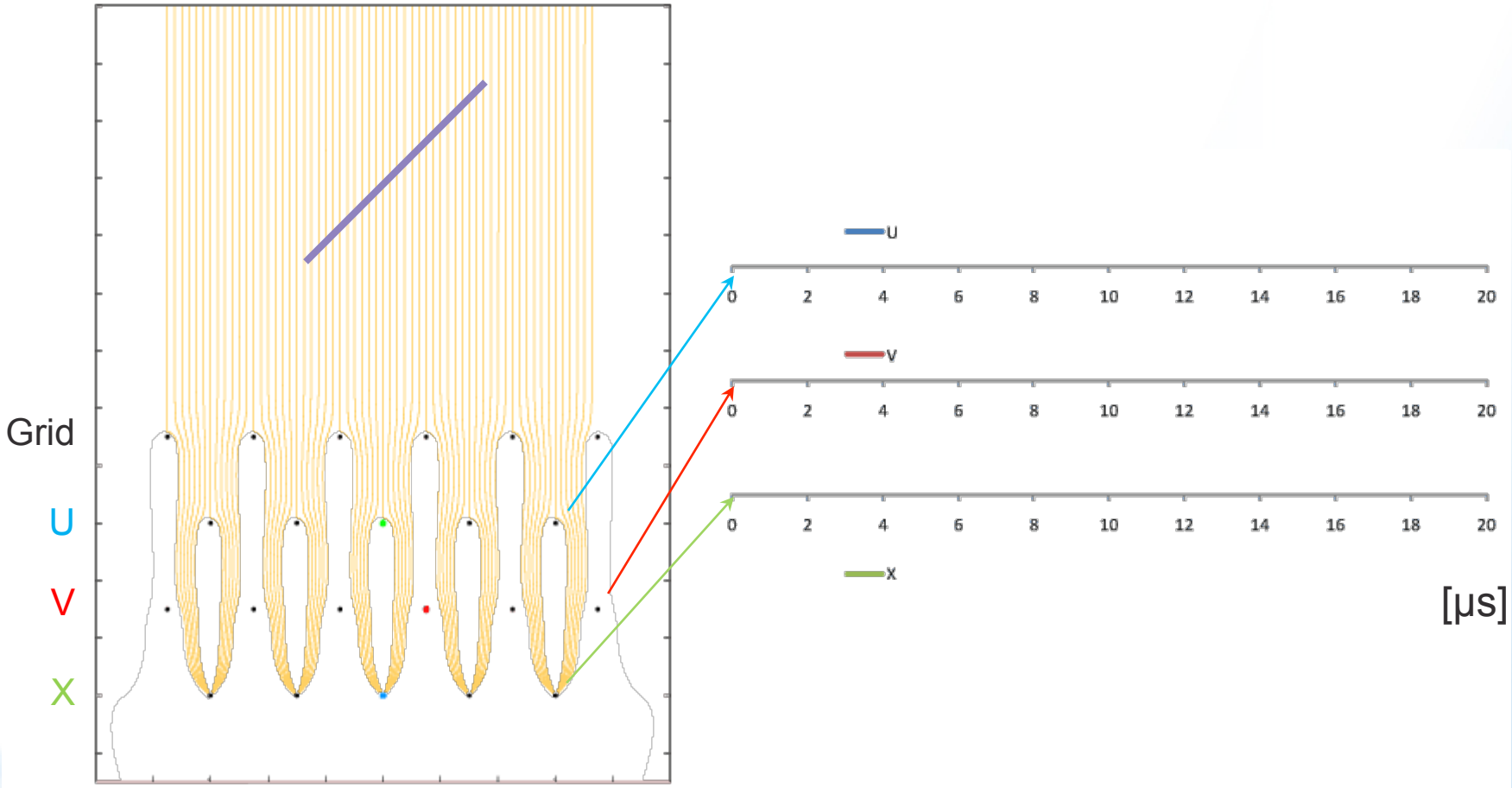
BROOKHAVEN NATIONAL LABORATORY
a passion for discovery

Office of Science
U.S. DEPARTMENT OF ENERGY

Outline

- **Readout Electronics Design Considerations**
  - **LAr TPC Signal Properties**
  - Necessity of Cold Electronics
  - CMOS Properties at Low Temperature
- Electronics Design in LAr TPC Experiments
  - MicroBooNE Project
  - LBNE Project and 35 Ton Prototype
  - LAr1 Proposal
- Summary

Signal Formation: Induced Signals from a Track Segment



LBNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian (~1/2 drift length) to mimic diffusion

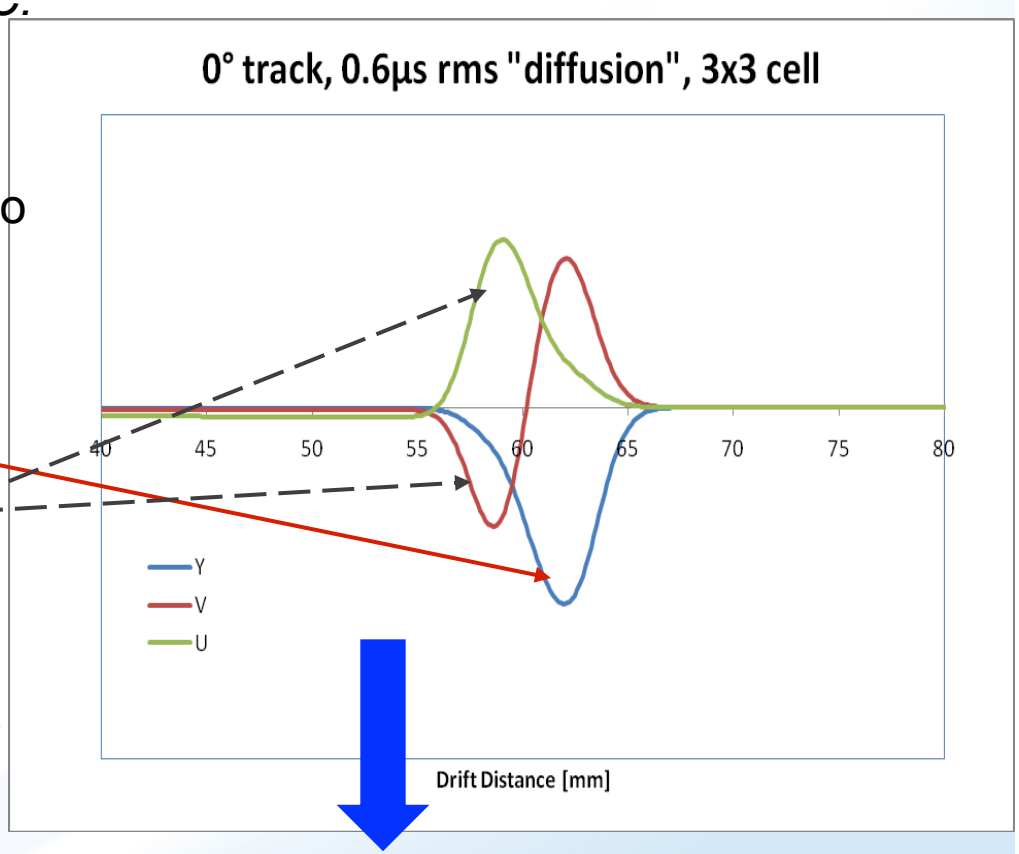
Signals in LAr TPC

Charge signal:

- A 3mm MIP track should create *210keV/mm x 3mm /23.6eV/e = 4.3fC.*
- After a 1/3 initial recombination loss: *~2.8fC*
- Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368.
- The expected signal for *3mm* wire spacing is then ≈*1fC=6250 e*, … and for *5mm, ≈10^4 e*, for ***the "collection signal"***.
- The induction signals are smaller

- The ***time scale*** of TPC signals is determined by the ***wire plane spacing*** and ***electron drift velocity***, *(~1.5 mm/μs at 500 V/cm)*.

Induced Current Waveforms on 3 Sense Wire Planes:



Sampling rate ***≤ 2 Ms/s***

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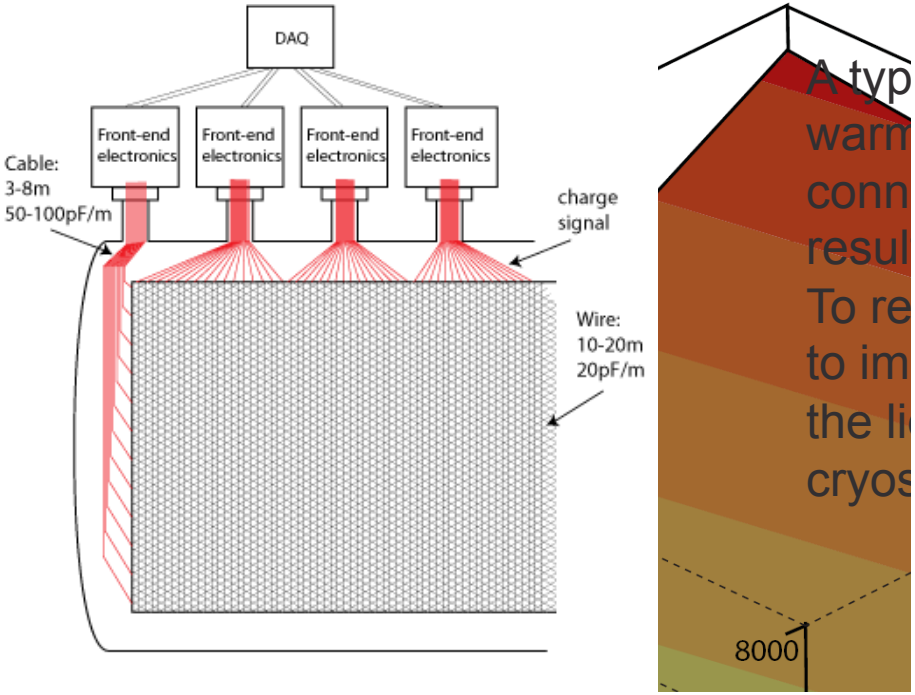
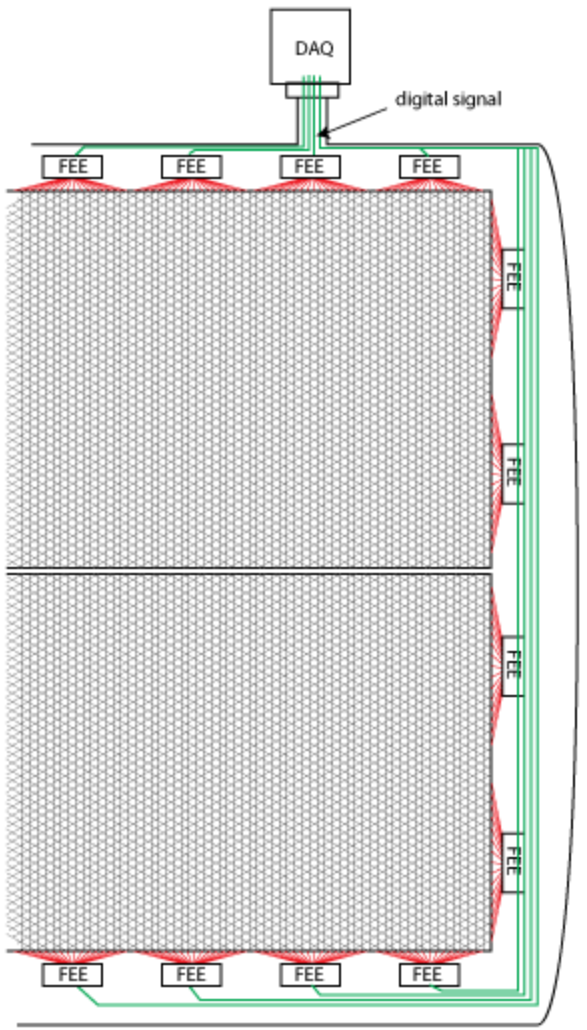
Advantages of Cold Electronics





Signal for drift)

5x5

Having front-end electronics in the cryostat, close to the wire electrodes yields the best SNR

Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations

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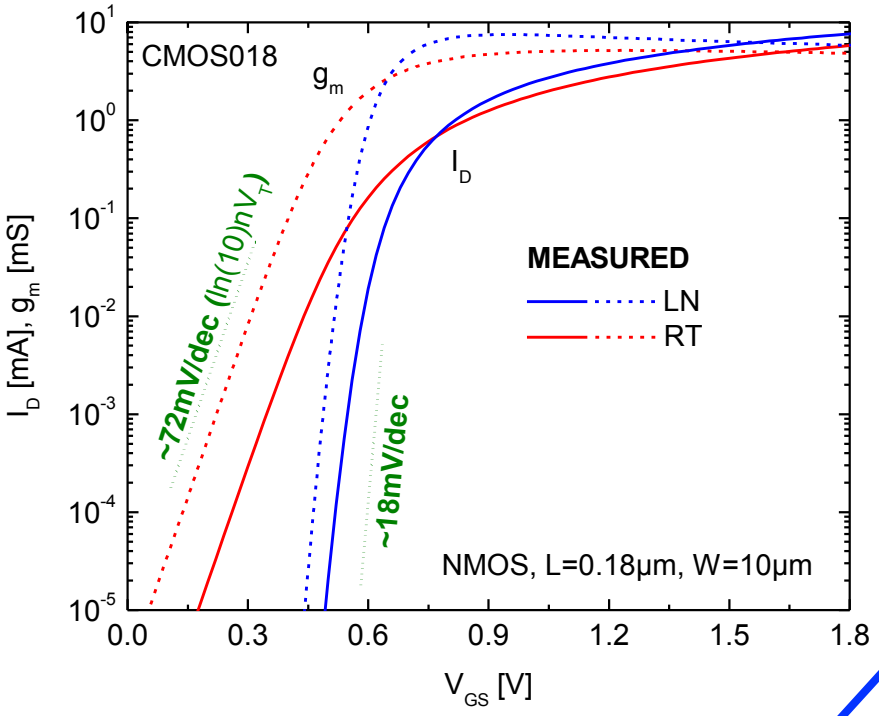
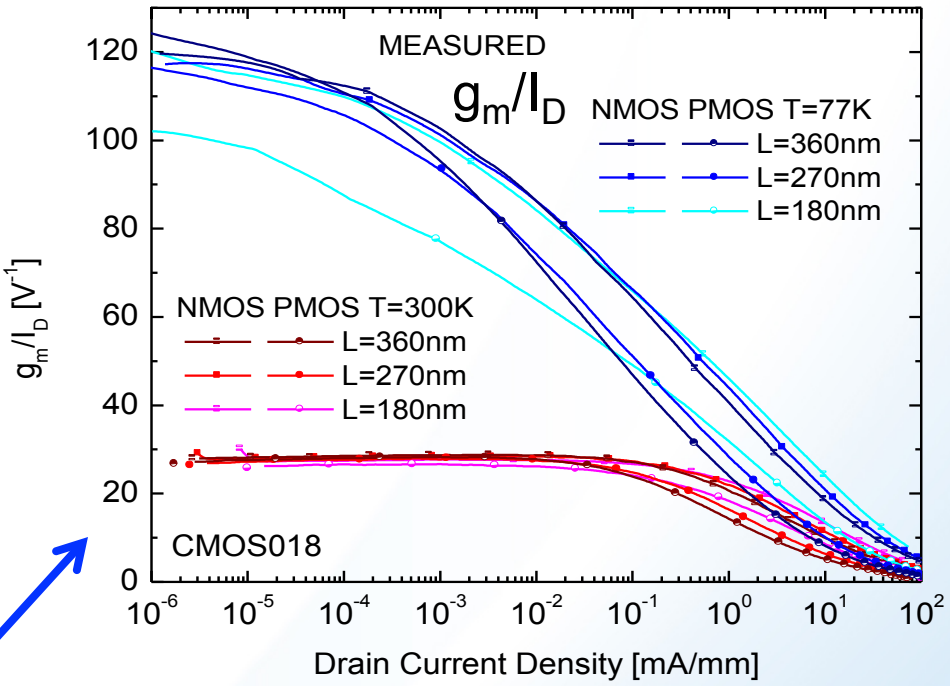
CMOS Characteristics in LAr



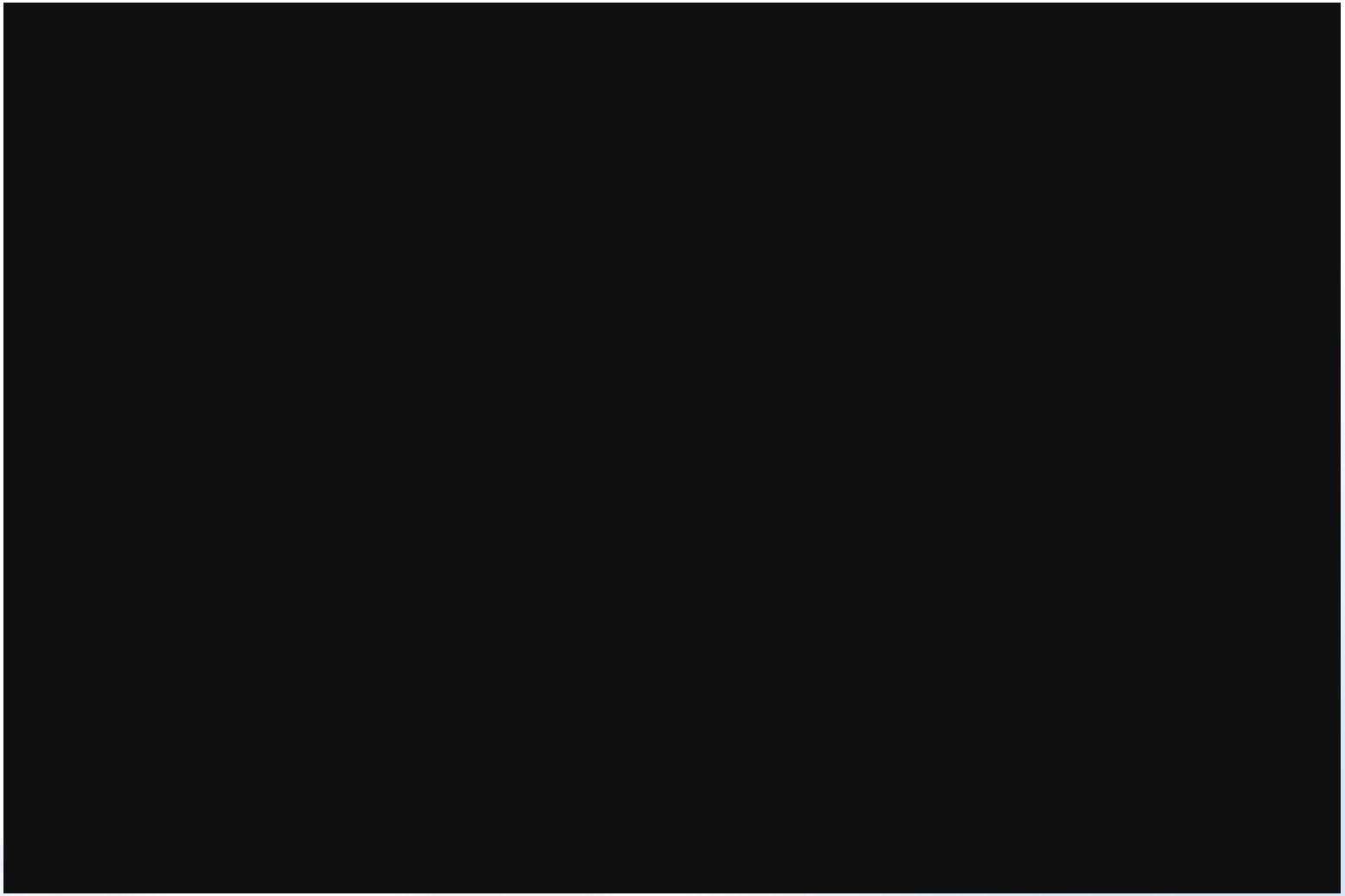


Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain, higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

Performance As ASIC Is Submerged in LN_2



If you have trouble viewing the video on Mac, download Flip4Mac

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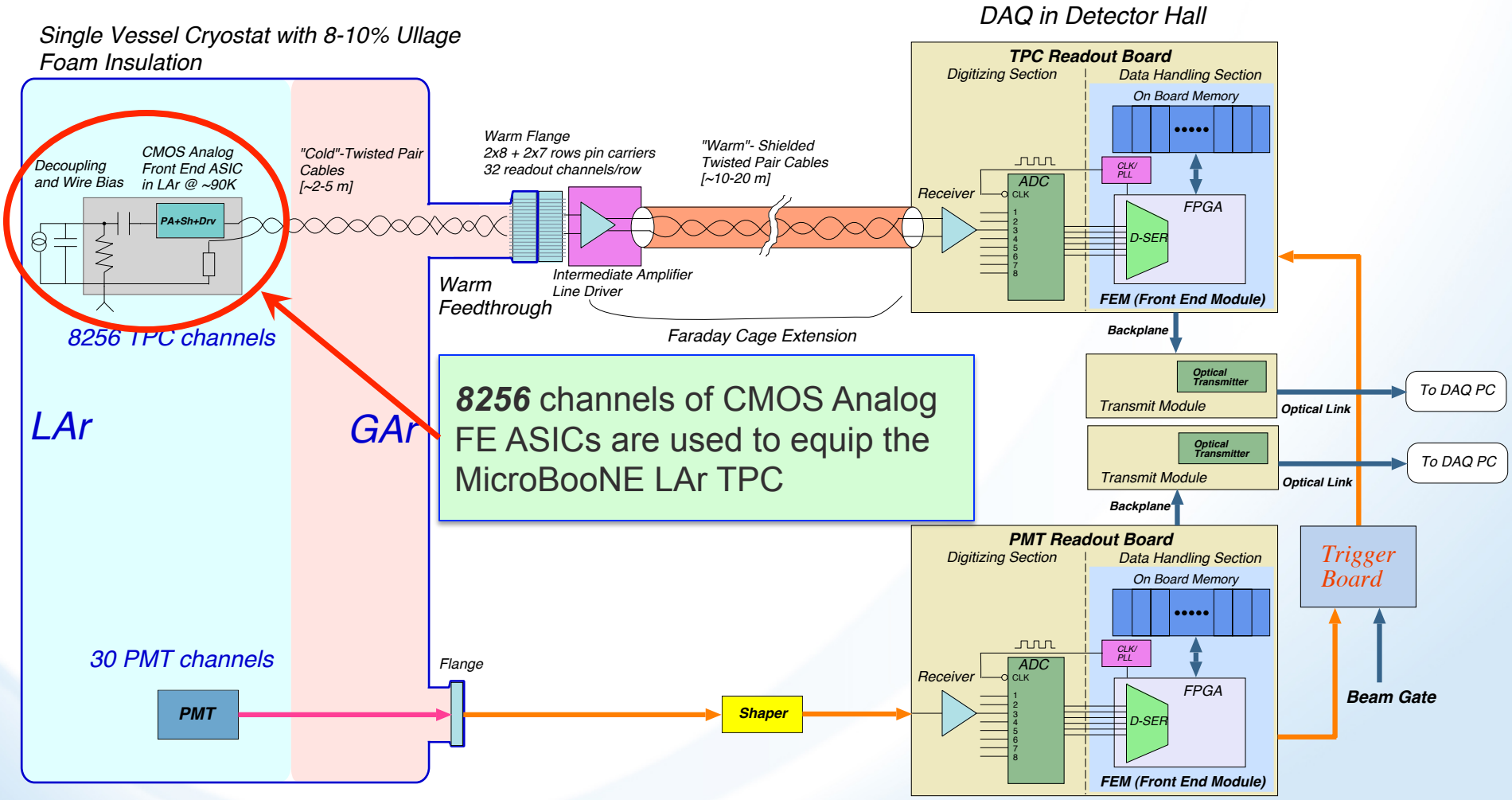
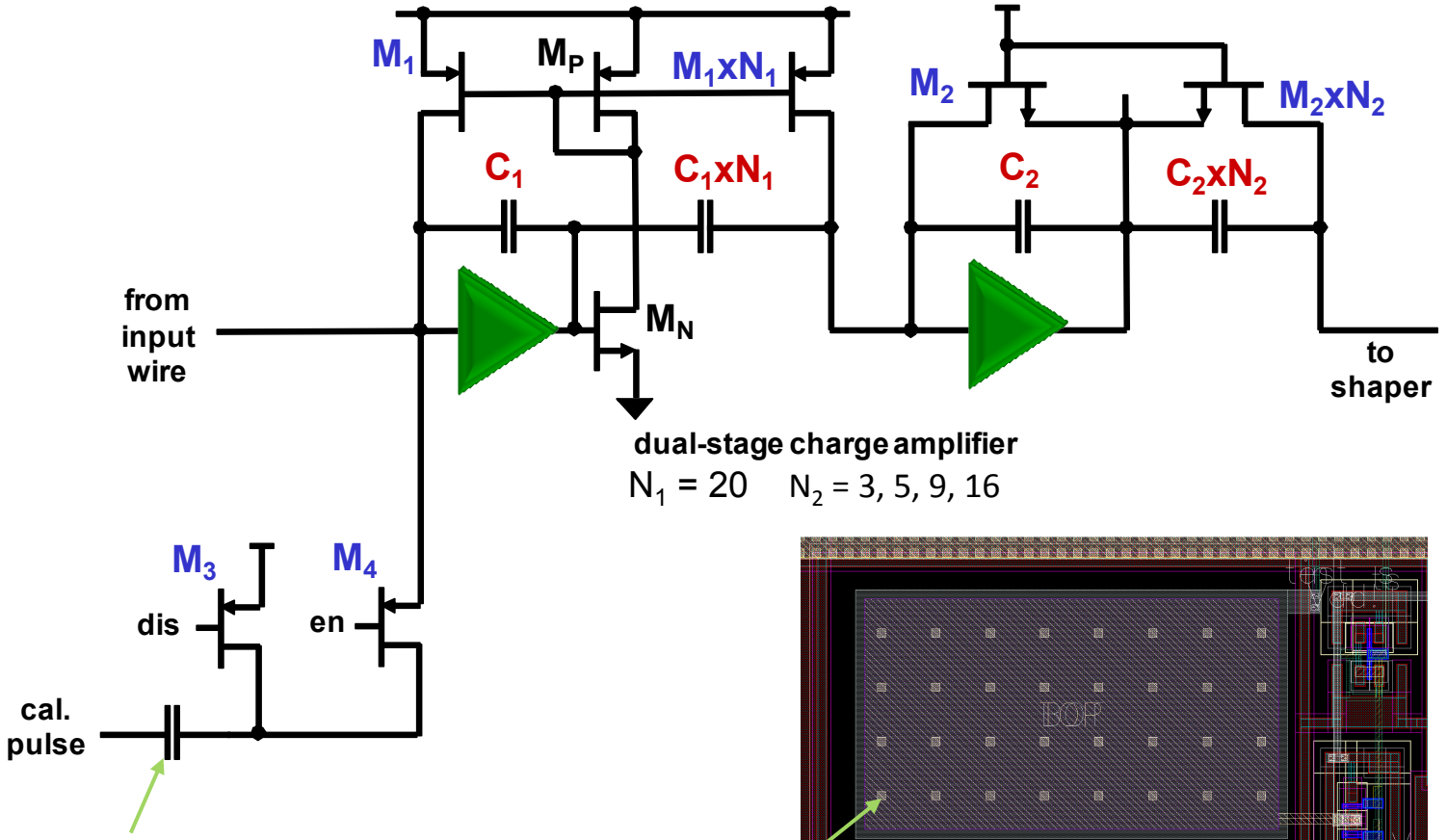
MicroBooNE Readout Electronics System



Cold Electronics ASIC - Front-End Detail and Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 μm²)

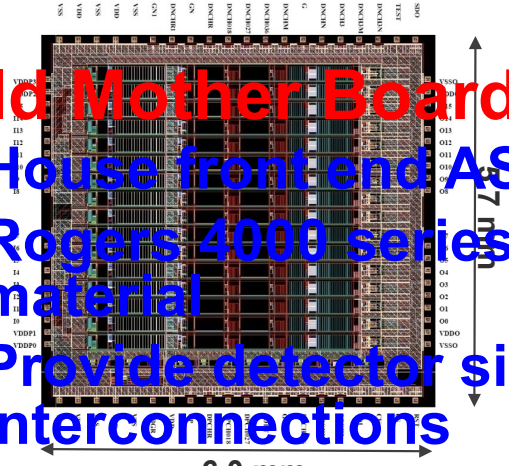
Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184\ fF\ \ at\ \ 300K \\ 183\ fF\ \ at\ \ 77K \end{cases}$$

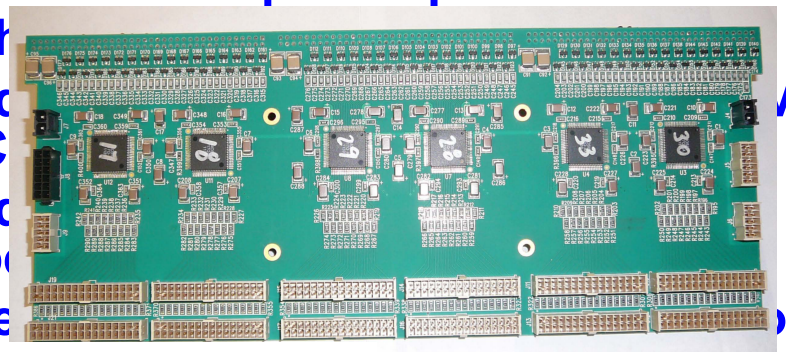
Charge sensitivity calibration of entire TPC during assembly, cooling and operation

MicroBooNE Cold Electronics

- **Cold Mother Board**
  - House front end ASIC
  - Rogers 4000 series base material
  - Provide detector signal interconnections
  - Provid… monito… networ…
  - Provid… distribu…
  - Horizo…
    - 96 "Y…
    - 48 "U…
    - 48 "V…
  - Vertica…
    - 96 "U…

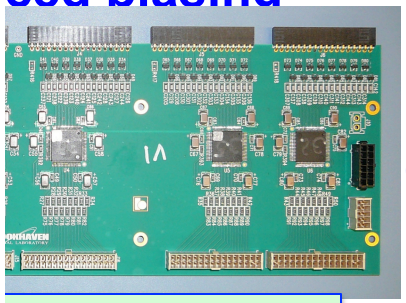


- **CMOS Analog Front End ASIC**
  - 16 channels per chip
  - Ch…
  - Ac… // fC
  - Ac… (p…
  - Se… …on



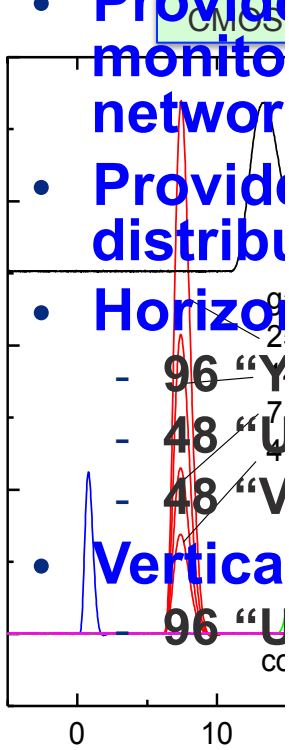
…motherboard with 12 …channels) populated

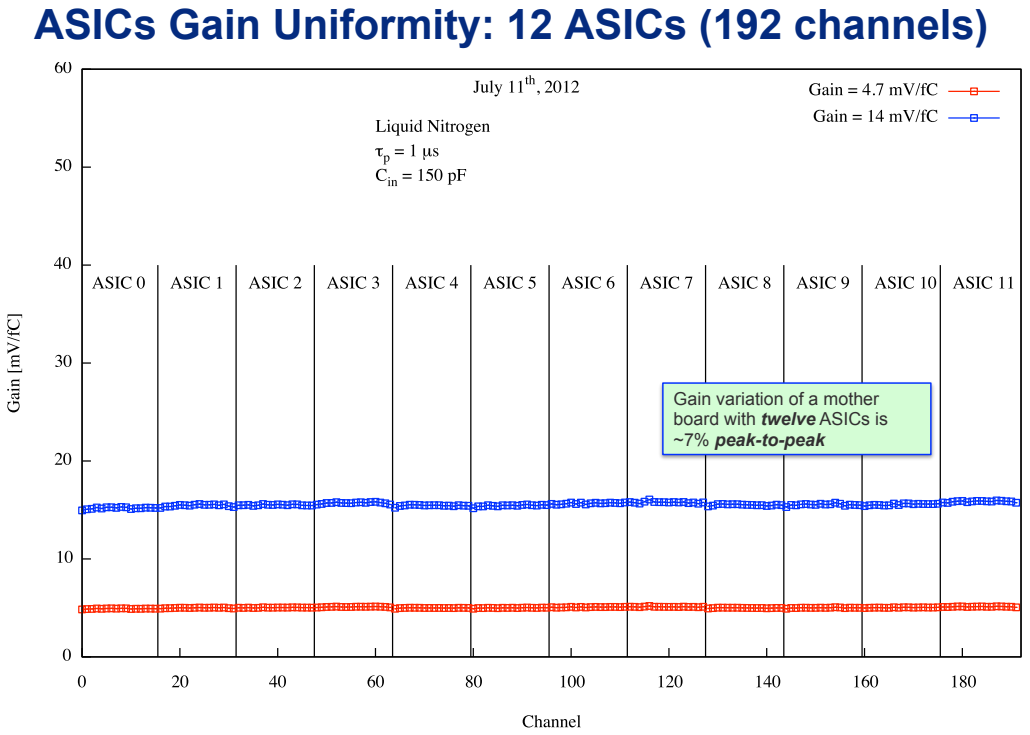
…ng
…signal processing
…ced biasing



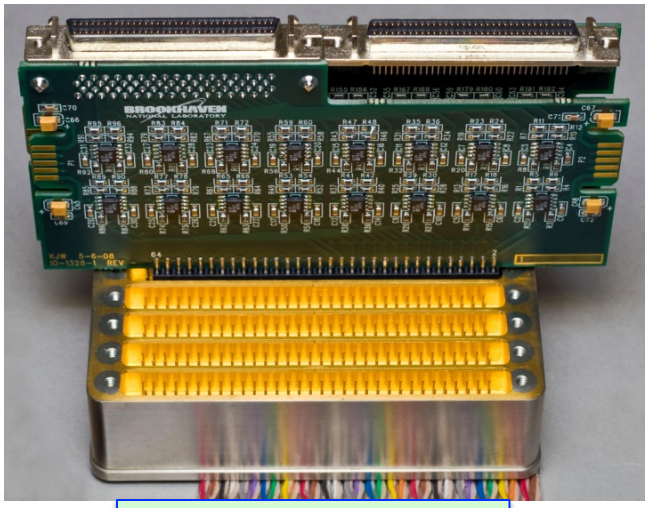
…6
…erboard with 6 ASIC …nnels) populated

…S 0.18 µm, 1.8 V,

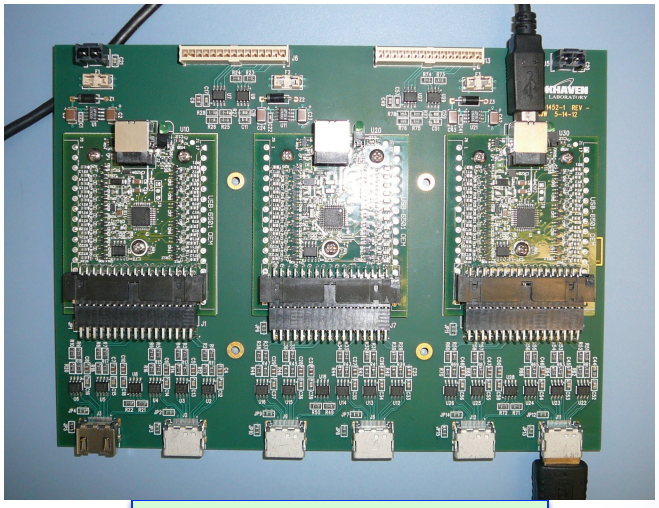




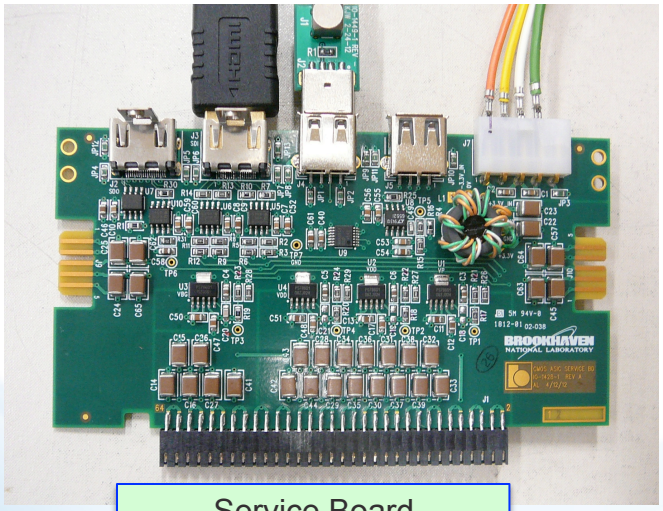
MicroBooNE Readout Electronics



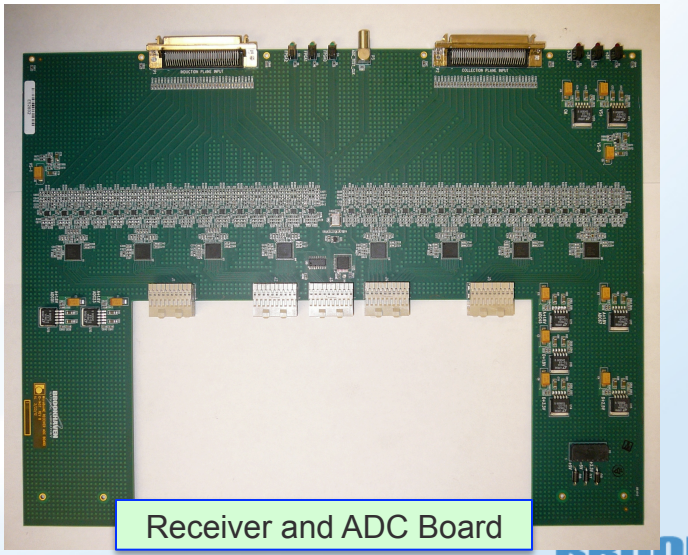
Intermediate Amplifier



ASIC Configuration Board



Service Board



Receiver and ADC Board

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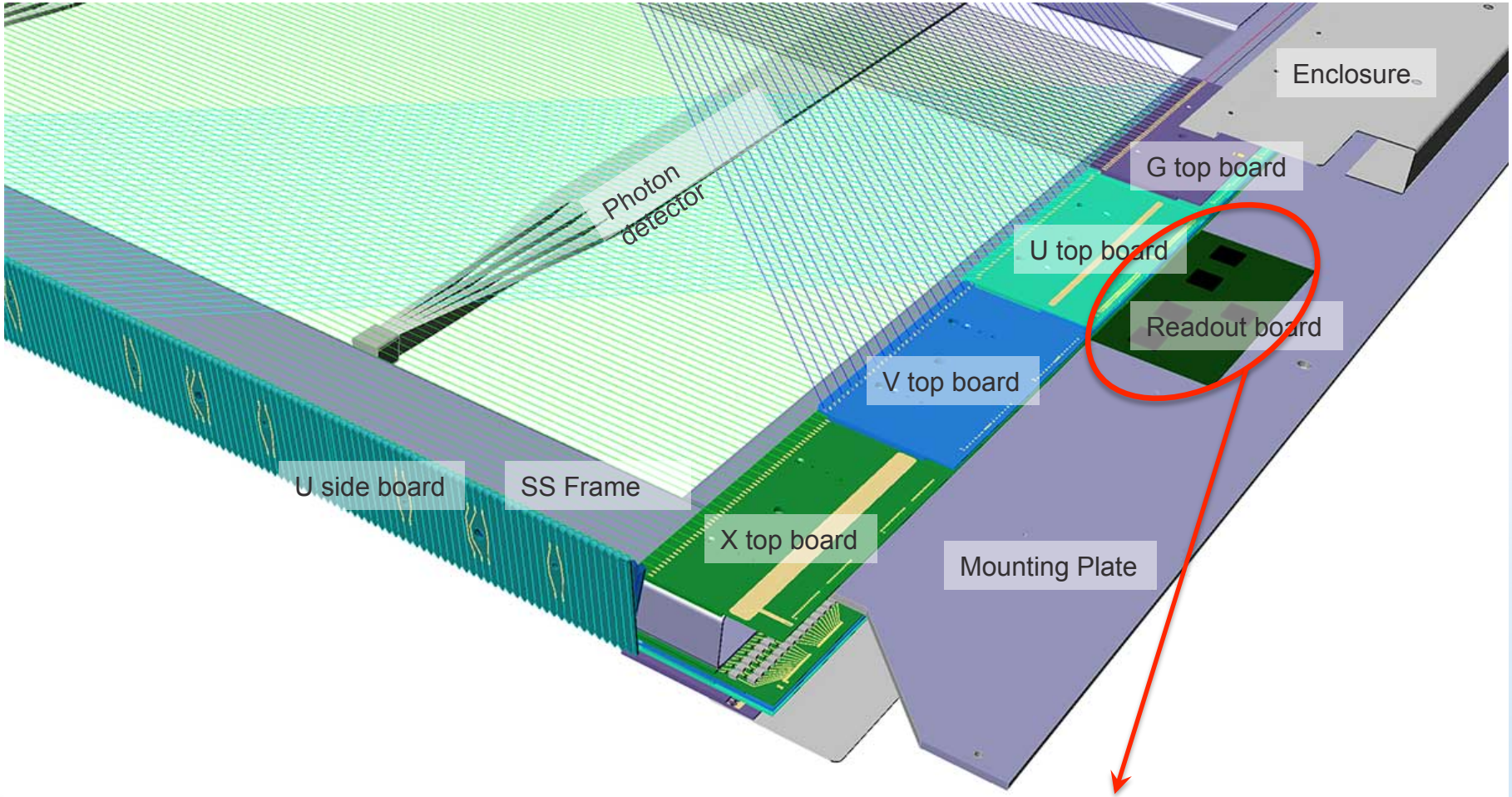
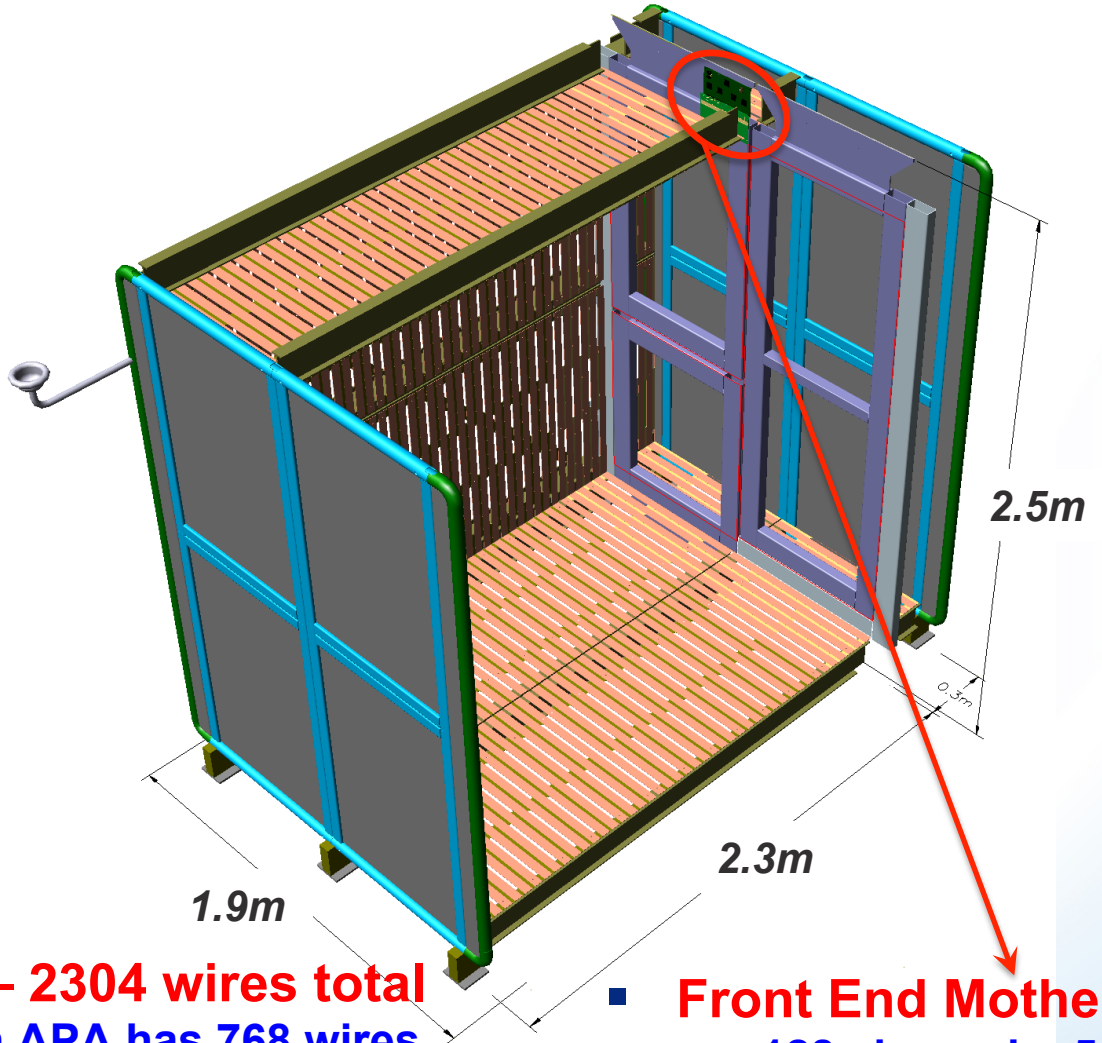
Cold Electronics for LBNE LAr TPC



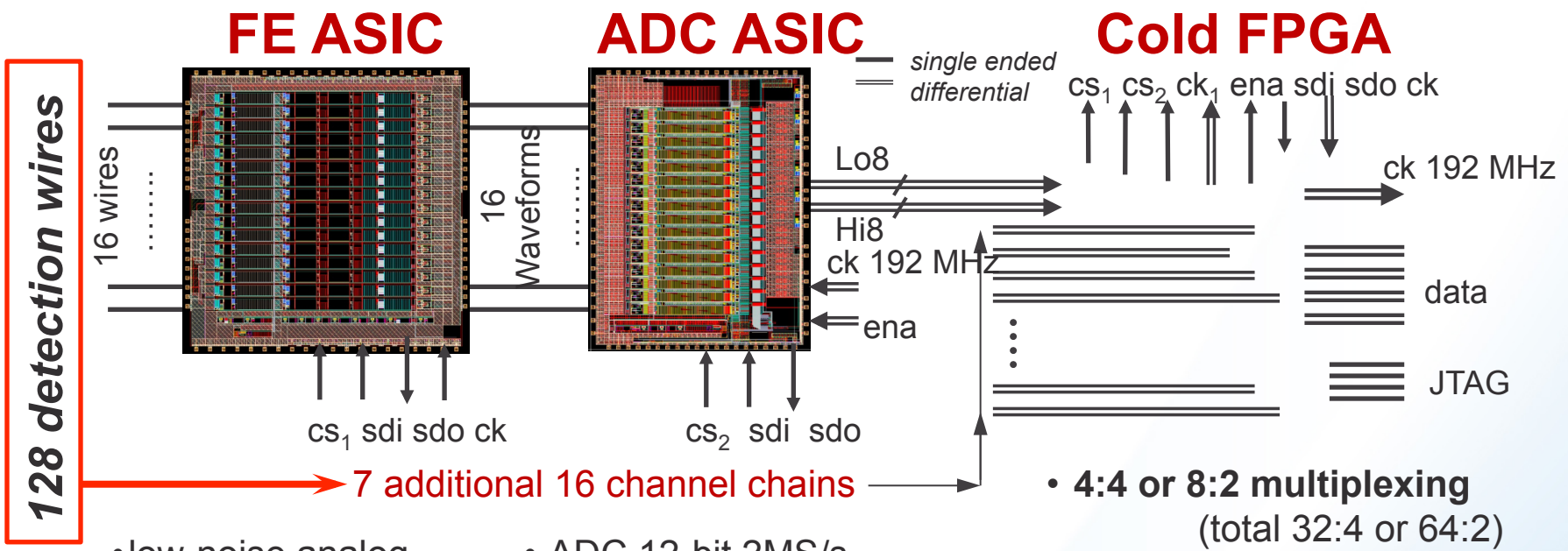
- **1 APA – 2560 wires**
  - 1120 X wires @ 4.5mm pitch
  - 720 U wires @ 4.9mm pitch
  - 720 V wires @ 5.0mm pitch
- **Front End Mother Board**
  - 128 channels: 56X, 36U,36V
  - 20 mother boards mounted on one end of the APA frame

Cold Electronics for 35T LAr TPC



- 3 APA – 2304 wires total
  - Each APA has 768 wires
  - 336 X wires @ 4.5mm pitch
  - 216 U wires @ 4.9mm pitch
  - 216 V wires @ 5.0mm pitch
- Front End Mother Board
  - 128 channels: 56X, 36U,36V
  - 6 mother boards mounted on one end of the APA frame

Key Components of Cold Electronics

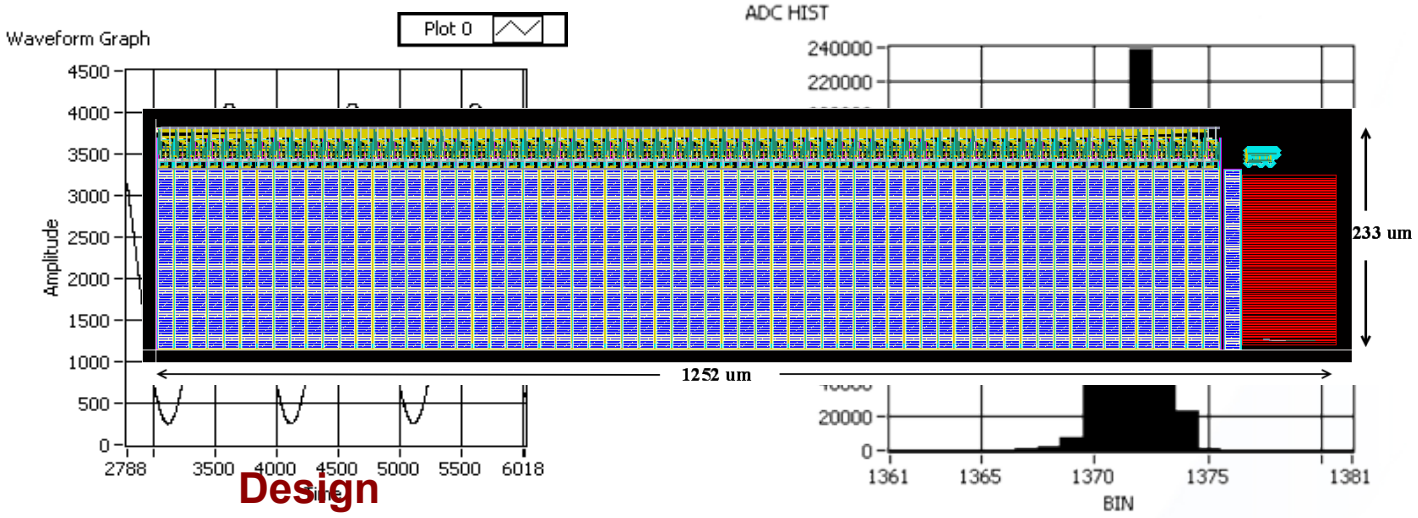


- low-noise analog amplification
- programmable gain, shaping, coupling, …
- charge calibration over all chips, channels and temperatures to 1%

- ADC 12-bit 2MS/s sampling rate
- built-in FIFO
- serialized outputs
- 2 x **8:1 multiplexing**

- **4:4 or 8:2 multiplexing** (total 32:4 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering
- ***support non-reduction transparent mode***
- ***max output data rate 960Mbit/s or 1.92Gbit/s with overhead of 8B/10B***

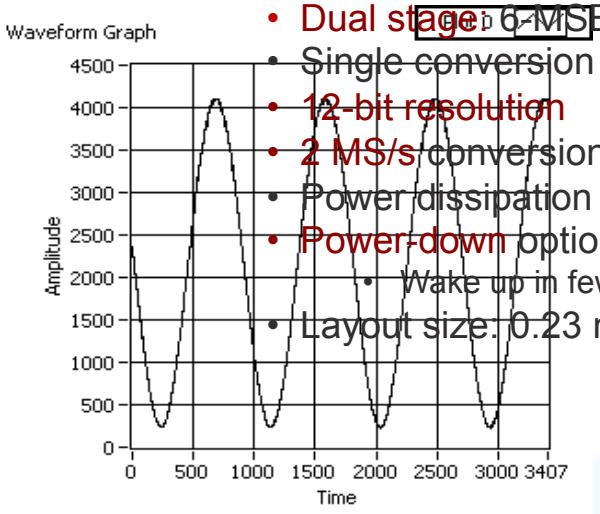
Single Cold ADC Test Results



Design

- Clockless low power current mode ADC
- Dual stage: 6-MSBs in 150ns, then 6-LSBs in 250ns
- Single conversion trigger per stage
- 12-bit resolution
- 2 MS/s conversion rate
- Power dissipation 3.6 mW at 2 MS/s
- Power-down option
  - Wake up in few tens of ns
- Layout size: 0.23 mm x 1.25 mm

Sinewave at RT



Sinewave at 77 K

ADC Output Histogram DC

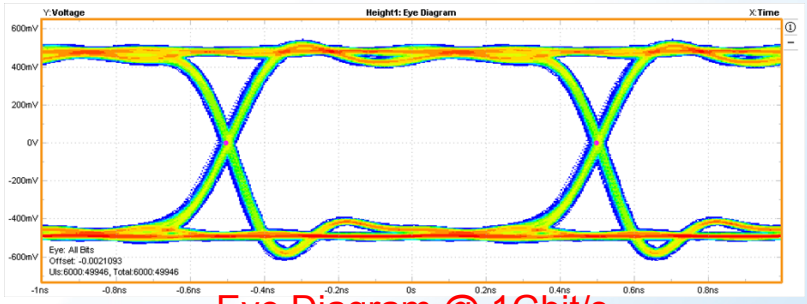
- **Measured linearity**
  - **DNL < 1.5 LSB for majority of codes**
  - **INL ~1% of Range**
- **Equivalent input noise measurement**
  - **1.27 LSB**
  - **Effective resolution wrt input referred noise: 11.6 bits**

The ADC has been tested with an FPGA, both immersed in LN_2

Cold FPGA Test

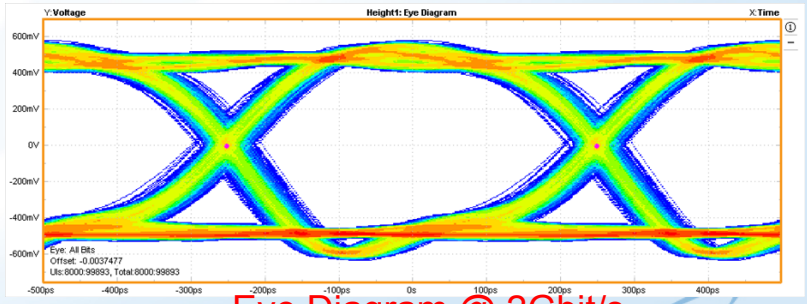
Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status	
ALTERA	Arria GX	90nm	3.125	4 - 12	1.2 - 4.5	1.2	Tested by BNL	✔
ALTERA	Arria II	40nm	6.375	8 - 24	2.9 - 16.4	0.9	Tested by BNL	✗
ALTERA	Stratix II GX	90nm	6.375	4 - 20	1.4 - 6.7	1.2	Tested by SMU	✔
ALTERA	Cyclone IV E	60nm	N/A	N/A	0.3 - 3.9	1.0, 1.2	Tested by BNL	✔
ALTERA	Cyclone IV GX	60nm	3.125	2 - 8	0.5 - 6.5	1.2	Tested by BNL	✔
ALTERA	Cyclone V GX	28nm	3.125	4 - 12	1.2 - 12.2	1.1	Test is ongoing	
XILINX	Virtex 5	65nm	6.5	0 - 24	0.9 - 18.6	1.0	Test is ongoing	

Cyclone IV GX Transceiver Starter Board



Eye Diagram @ 1Gbit/s

- **Test of Cyclone IV GX Transceiver Starter Board in LN_2**
  - **Transceiver works well at both 1Gbit/s and 2Gbit/s**
  - **JTAG configuration works**
  - **AS configuration works with Altera EPCS device**
  - **Internal memory works with SignalTap**
  - **Internal PLL and fabric work for clock generation**
  - **On board SRAM works with BIST**



Eye Diagram @ 2Gbit/s

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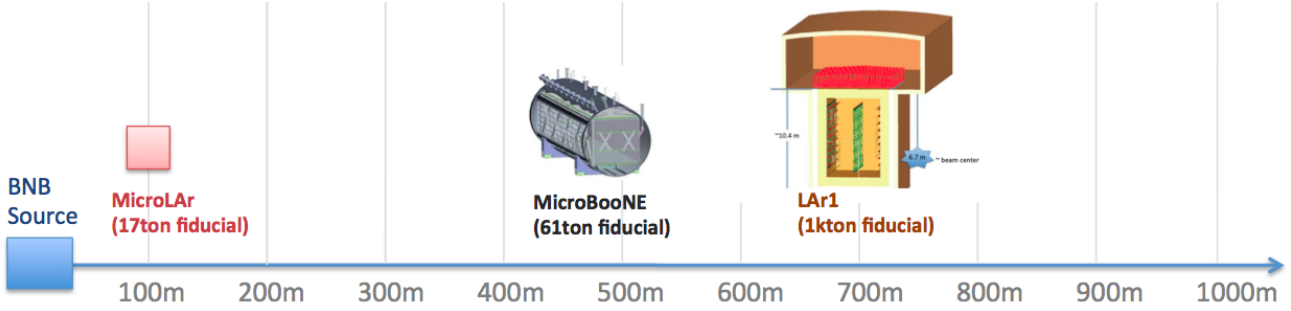
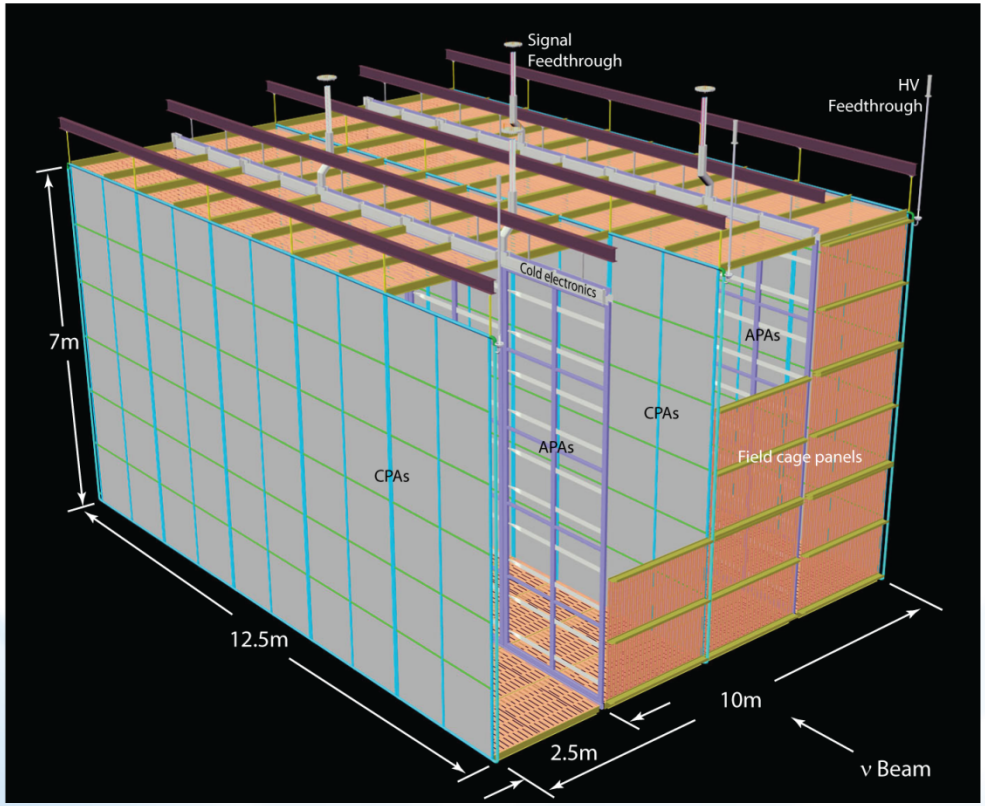
LAr1 Proposal (In Preparation)





Conceptual design of LAr1-FD TPC inside the cryostat

- **LAr1 is a proposal for a neutrino oscillation experiment on the booster neutrino beam**
  - Multiple LArTPCs to address the anti-neutrino short baseline anomalies and provide development input for very large LArTPC detectors for long baseline oscillation physics
  - LAr1-ND at 100 m
  - MicroBooNE at 470 m
  - LAr1-FD at 700 m
- **Design of LAr1 detector relies heavily on and is the evolution of many years of generic detector R&D and work done on MicroBooNE and LBNE**

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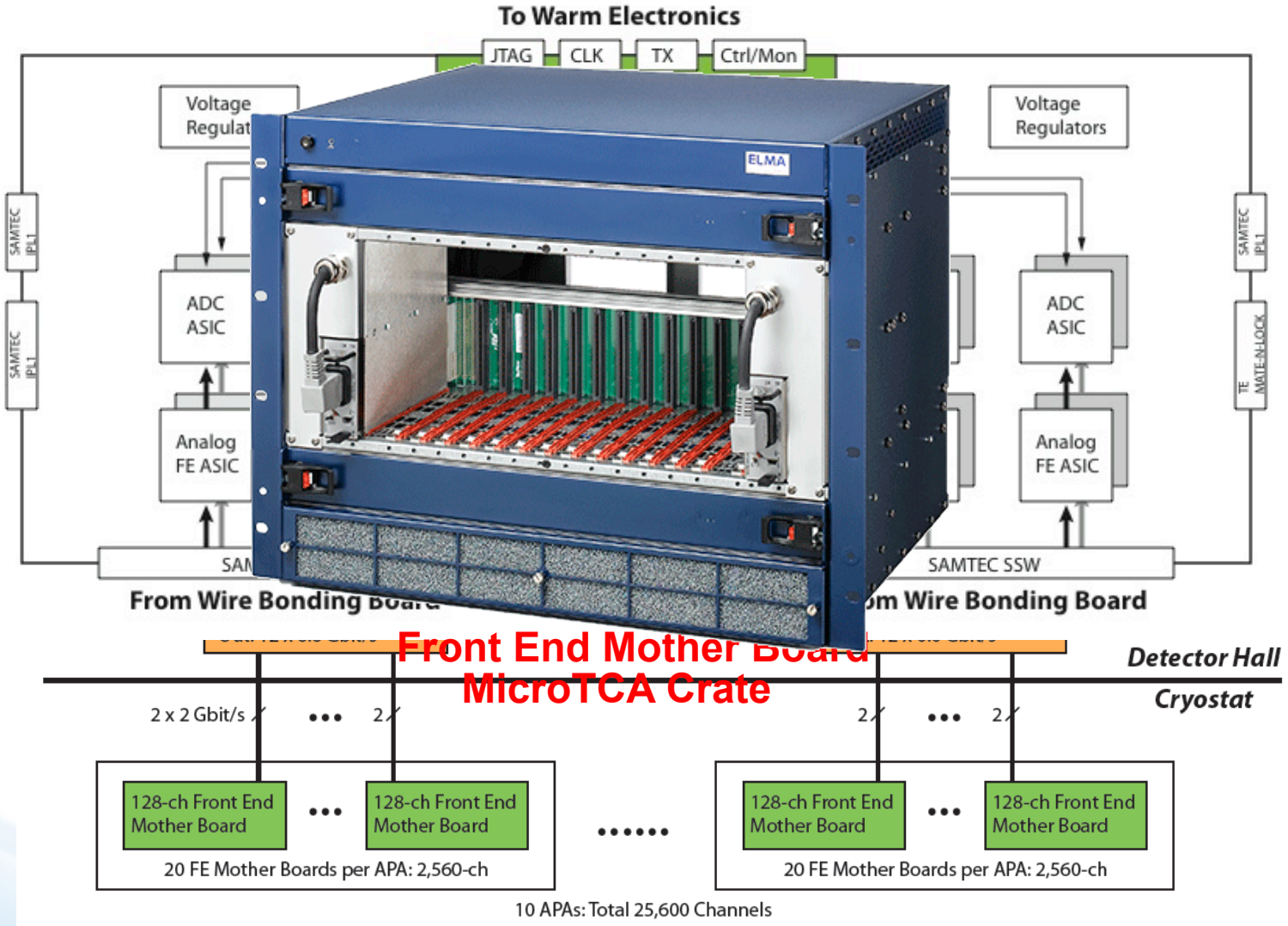
Readout Electronics of LAr1-FD



Summary

- **Cold electronics installed directly on the detector electrodes is critical to make possible giant LAr TPCs and improve signal to noise ratio**
- **CMOS at Low Temperature**
  - **Started from .18um CMOS technology with only 300K models for analog front end; parameters extracted at 77K**
  - **CMOS found functioning at cryogenic temperature with *increased* gain (g_m/I_{ds}) and *lower* noise**
- **Development of Readout Electronics for LAr TPC**
  - **We have accumulated *~2,000 chip•immersions* of analog FE ASIC in LN_2 without any failures due to thermal contraction/expansion**
  - **ADC characterization test and cold FPGA lifetime study are being conducted**
  - **Analog FE ASIC + ADC ASIC + Cold FPGA will be used to equip the 35 Ton LAr TPC and LAr1 Far Detector**